PCISA-C3/EDEN

VIA® Processor CPU Board with 10/100Mb LAN & VGA

User Manual

Version 1.3

December 1, 2003

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Chapter 1. Introduction

The PCISA-C3/EDEN SERIES ATX/AT main board is a high-performance computer mainboard based on the VIA® Apollo PLE133 VT8601A and VT82C686B chipset. It is designed for VIA® C3 processor, making it ideal for cost-effective CPU board markets.

The VIA® Apollo PLE133 (VT8601A) is a VIA® C3 processor system logic north bridge with the addition of 133 MHz capability for both the CPU and SDRAM interfaces. VIA® Apollo PLE133 may be used to implement both desktop and notebook personal computer systems from 100MHz to 133MHz based on C3 (EBGA packing). The primary features of the VIA® Apollo PLE133-North Bridge are: VIA® C3 CPU (Front Side Bus) Interface (100 / 133MHz), SDRAM Memory Interface (100 / 133MHz), 32-bit PCI with Integrated 2D / 3D graphics accelerator.

The VT82C686B PSIPC (PCI Super-I/O Integrated Peripheral Controller) is a high integration, high performance, power-efficient, and high compatibility device that supports both Intel and non-Intel based processors to PCI bus bridge functionality, ensuring a complete Microsoft PC99-compliant PCI/ISA system.

1.1 Specifications

- **VIA® C3 EBGA packing (FSB: Supports 100/133MHz)**
- **Bus**: PICMG Bus (Support PCI Master x 4)
- **DMA channels**: 7
- **Interrupt levels**: 15
- **Chipset**: VIA® VT8601A (Integrated 2D / 3D graphics accelerator.) & VT82C686B
- **RAM memory**:
  - ✓ One 168-pin DIMM sockets.
  - ✓ Maximum memory is 512MB.
- **Ultra ATA/33/66/100 IDE Interface** : Two PCI Enhance IDE hard drives. The south bridge VT82C686B supports Ultra ATA/33/66/100 IDE interface.
- **Floppy disk drive interface** : Supports 2.88 MB, 1.44MB, 1.2MB, 720KB, or 360KB floppy disk drive.
- **Two high speed serial ports** : NS16C550 compatible UART's
- **Bi-directional parallel port** : IEEE1284 compatible
- **IrDA port :** Supports Serial Infrared(SIR) and Amplitude Shift Keyed IR(ASKIR) interface.
- **USB port :** Equipped with four USB ports for future expansion.
- **Intel 82559 or REALTEK RTL8100 Fast Ethernet Multifunction PCI Controller :**
  - ✓ IEEE 802.3u Auto-Negotiation support for 10BASE-T/100BASE-TX standard.
  - ✓ Fast back-to-back transmission support with minimum interface spacing.
  - ✓ Connected to your LAN via RJ45 connector.

- **Keyboard connector & PS/2 Mouse Port on-board**
- **Power Consumption** : +5VSB @ 180mA, +5V @ 3.8A, +12V @ 170mA (C3-800MHz with 512MB SDRAM x 2, Windows2000)
- **Operating Temperature** : 0◦ ~ 55◦ C (CPU needs Cooler)

1.2 Package Contents

In addition to this *User's Manual*, the PCISA-C3/EDEN SERIES package includes the following items:

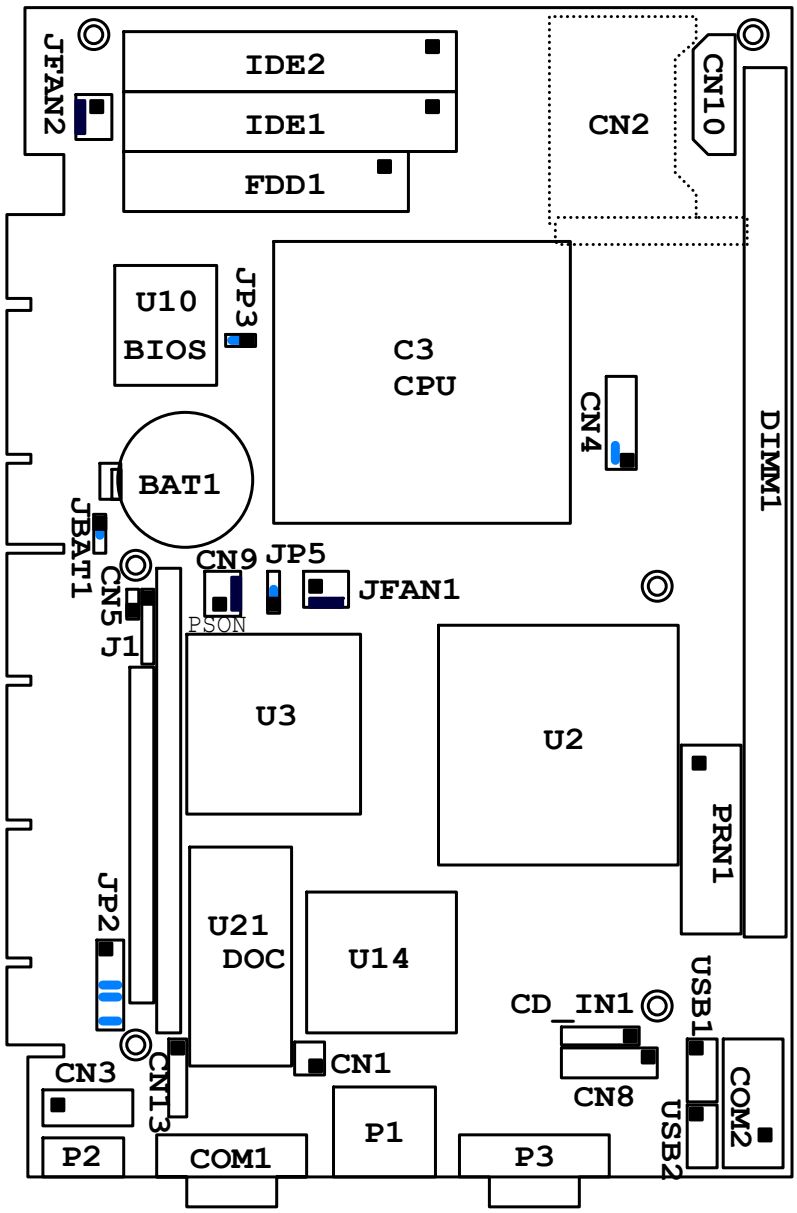
- PCISA-C3/EDEN SERIES Single Board Computer x1
- IDE HDD Cable x 1
- FDD Cable x 1
- RS-232/Print Cable x 1
- Y Cable x 1
- Audio Cable x 1
- RS-422/485 Cable x 1
- CD-ROM Driver x 1

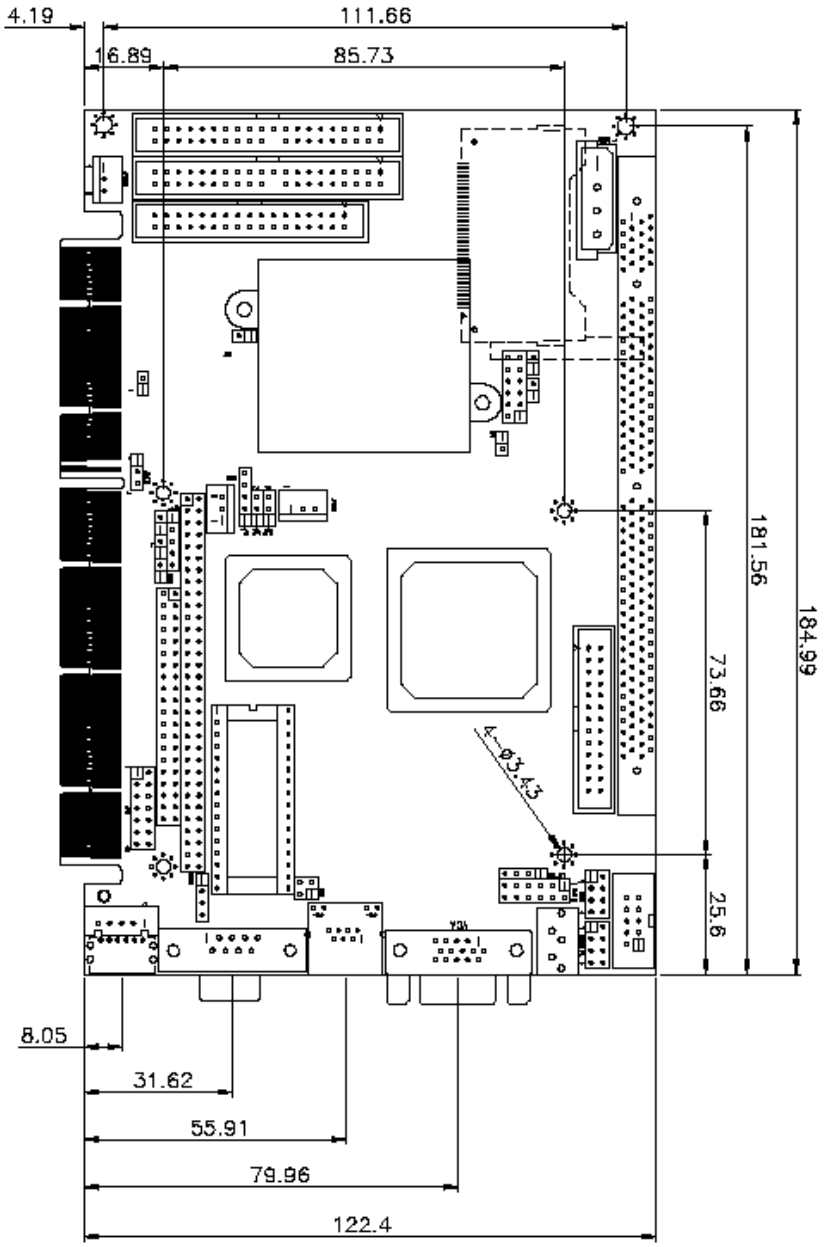
If any of these items are missing or damaged, please contact the dealer from whom you purchased the product. Be sure to save the shipping materials and carton in case you want to ship or store the product in the future.

Chapter 2. Installation

This chapter describes how to install the PCISA-C3/EDEN SERIES. First a layout diagram of the PCISA-C3/EDEN SERIES is shown, followed by unpacking information that should be carefully followed. The jumpers and switch settings for the PCISA-C3/EDEN SERIES configuration, such as CPU type selection, system clock setting, and watchdog timer, are also listed.

2.1 Layout Diagram & Dimensions

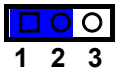



4.19
111.66
16.89
85.73
181.56
184.99
73.66
25.6
4-Φ3.43
8.05
31.62
55.91
79.96
122.4

2.2 Clear CMOS Setup

To clear the CMOS Setup (for example if you have forgotten the password, you should clear the CMOS and then re-set the password), you should close the JBAT1 (2-3) for about 3 seconds, then open it once more. This will set back to normal operation mode.

- **JBAT1 : Clear CMOS Setup**



JBAT1	DESCRIPTION
1-2 (default)*	Keep CMOS Setup (Normal Operation)
Short 2-3	Clear CMOS Setup

2.3 Compact Flash Card Master/Slave Mode Setting

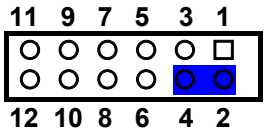
The Compact Flash socket is type II, and uses IDE 2.

- **JP3 : Master/Slave Mode Setting**

JP3	DESCRIPTION
SHORT *	MASTER
OPEN	SLAVE

2.4 Buzzer Function Setting

- **CN4(2-4) : Enabled/Disabled Onboard Buzzer Function**

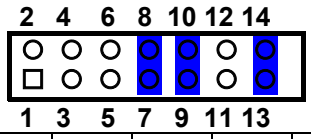


2 - 4	DESCRIPTION
SHORT *	Enabled
OPEN	Disabled

2.5 DiskOnChip™ Flash Disk Memory Address Setting

The DiskOnChip™ Flash Disk Chip (DOC) is produced by M-Systems. Because the DOC is 100% compatible with the hard disk, no extra software utilities are required. It is, in other words, "plug and play" - easy and reliable. At the present time, the DOC is available with between 2MB and 144MB.**The MD-2200-Xmb series DOC will share only 8KB memory address.**

- **JP2: DiskOnChip Memory Address Settings**



ADDRESS	1-2	3-4	5-6	7-8	9-10	11-12	13-14
CC000	OPEN	OPEN	CLOSE	OPEN	OPEN	CLOSE	CLOSE
CE000	OPEN	OPEN	OPEN	CLOSE	OPEN	CLOSE	CLOSE
D0000	CLOSE	OPEN	OPEN	OPEN	CLOSE	OPEN	CLOSE
D2000	OPEN	CLOSE	OPEN	OPEN	CLOSE	OPEN	CLOSE
D4000	OPEN	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
D6000	OPEN	OPEN	OPEN	CLOSE	CLOSE	OPEN	CLOSE
D8000	CLOSE	OPEN	OPEN	OPEN	OPEN	OPEN	CLOSE
DA000	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN	CLOSE
DC000	OPEN	OPEN	CLOSE	OPEN	OPEN	OPEN	CLOSE
DE000	OPEN	OPEN	OPEN	CLOSE	OPEN	OPEN	CLOSE

2.6 COM2 RS232 or RS422/485 Selection

- **JP5 : COM2 RS232 or RS422/485 Selection**

JP5	DESCRIPTION
1-2 Short	RS232
2-3 Short	RS422/485

Caution: *If RS422/485 is in use, the COM2 on the main board would be disable.*

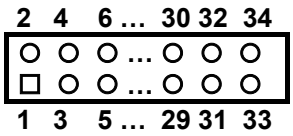
Chapter 3. Connection

This chapter describes how to connect peripherals, switches and indicators to the PCISA-C3/EDEN SERIES board.

3.1 Floppy Disk Drive Connector

PCISA-C3/EDEN SERIES board is equipped with a 34-pin daisy-chain driver connector cable.

- **FDD1 : FDC CONNECTOR**



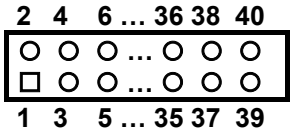
PIN	DESCRIPTION	PIN	DESCRIPTION
1	GROUND	2	REDUCE WRITE
3	GROUND	4	N/C
5	GROUND	6	N/C
7	GROUND	8	INDEX#
9	GROUND	10	MOTOR ENABLE A#
11	GROUND	12	DRIVE SELECT B#
13	GROUND	14	DRIVE SELECT A#
15	GROUND	16	MOTOR ENABLE B#
17	GROUND	18	DIRECTION#
19	GROUND	20	STEP#
21	GROUND	22	WRITE DATA#
23	GROUND	24	WRITE GATE#
25	GROUND	26	TRACK 0#
27	GROUND	28	WRITE PROTECT#
29	N/C	30	READ DATA#
31	GROUND	32	SIDE 1 SELECT#
33	N/C	34	DISK CHANGE#

3.2 PCI E-IDE Disk Drive Connector

You can attach up to four IDE(Integrated Device Electronics) devices.

IDE1 : Primary IDE Connector
IDE2 : Secondary IDE Connector

- **IDE1 / IDE2 : IDE Interface Connector**

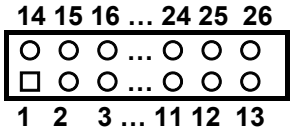


PIN	DESCRIPTION	PIN	DESCRIPTION
1	RESET#	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	N/C
21	DRQ	22	GROUND
23	IOW#	24	GROUND
25	IOR#	26	GROUND
27	CHRDY	28	REV. PULL LOW
29	DACK	30	GROUND-DEFAULT
31	INTERRUPT	32	N/C
33	SA1	34	N/C
35	SA0	36	SA2
37	HDC CS0#	38	HDC CS1#
39	HDD ACTIVE#	40	GROUND

3.3 Parallel Port

Usually, a printer is connected to the parallel port. The PCISA-C3/EDEN SERIES includes an on-board parallel port, accessed via a 26-pin flat-cable connector PRN1.

- **PRN1 : Parallel Port Connector**

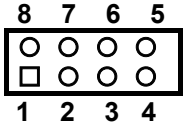


PIN	DESCRIPTION	PIN	DESCRIPTION
1	STROBE#	2	DATA 0
3	DATA 1	4	DATA 2
5	DATA 3	6	DATA 4
7	DATA 5	8	DATA 6
9	DATA 7	10	ACKNOWLEDGE
11	BUSY	12	PAPER EMPTY
13	PRINTER SELECT	14	AUTO FORM FEED #
15	ERROR#	16	INITIALIZE
17	PRINTER SELECT LN#	18	GROUND
19	GROUND	20	GROUND
21	GROUND	22	GROUND
23	GROUND	24	GROUND
25	GROUND	26	NC

3.4 USB Port Connectors

The PCISA-C3/EDEN SERIES is equipped with two USB(Version. 1.1) ports for the future new I/O bus expansion.

USB1 / USB2 : 4 ports USB Connector
USB1 / USB2 Pin 8,7,6,5 for PORT 3 / 1
USB1 / USB2 Pin 1,2,3,4 for PORT 2 / 0



PIN	DESCRIPTION	PIN	DESCRIPTION
1.	VCC	8.	GROUND
2.	DATA1-	7.	DATA0+
3.	DATA1+	6.	DATA0-
4.	GROUND	5.	VCC

3.5 Power Button Switch

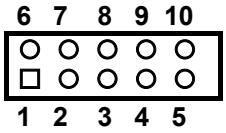
- **CN5 : 2 Pin Power Button Switch**

PIN	DESCRIPTION
2	Power Button
1	Ground

3.6 Serial Ports

The PCISA-C3/EDEN SERIES offers two high speed NS16C550 compatible UARTs with 16-byte Read/Receive FIFO serial ports.

- **COM1 / COM2 : Serial Port 10-pin Connector**



PIN	DESCRIPTION	
1	DATA CARRIER DETECT	(DCD)
2	RECEIVE DATA	(RXD)
3	TRANSMIT DATA	(TXD)
4	DATA TERMINAL READY	(DTR)
5	GROUND	(GND)
6	DATA SET READY	(DSR)
7	REQUEST TO SEND	(RTS)
8	CLEAR TO SEND	(CTS)
9	RING INDICATOR	(RI)
10	N/C	

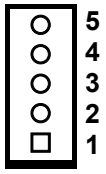
3.7 Keyboard/Mouse Connector

The PCISA-C3/EDEN SERIES has a 6-pin DIN keyboard/mouse connector and a 5-pin keyboard connector..

- **P2 : 6-pin DIN Keyboard/Mouse Connector**

PIN	DESCRIPTION
1	KEYBOARD DATA
2	MOUSE DATA
3	GROUND
4	+5V
5	KEYBOARD CLOCK
6	MOUSE CLOCK

- **CN3 : 5-pin External Keyboard Connector**

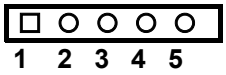


PIN	DESCRIPTION
1	KEYBOARD CLOCK
2	KEYBOARD DATA
3	NC
4	GROUND
5	+5V

3.8 IrDA Infrared Interface Port

The PCISA-C3/EDEN SERIES comes with an integrated IrDA port which supports either a Serial Infrared(SIR) or an Amplitude Shift Keyed IR(ASKIR) interface. When using the IrDA port, please ensure that COM2 is set in SIR or ASKIR mode in the BIOS's Peripheral Setup so that RS-232 mode on COM2 is disabled.

- **J1 : IrDA connector**

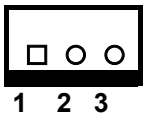


PIN	DESCRIPTION
1	VCC
2	N/C
3	IR-RX
4	Ground
5	IR-TX

3.9 Fan Connector

The PCISA-C3/EDEN SERIES also has a CPU with cooling fan connector and chassis fan connector, which can supply 12V/500mA to the cooling fan. There is a "rotation" pin in the fan connector, which transfers the fan's rotation signal to the system BIOS in order to recognize the fan speed. Please note that only specific fans offer a rotation signal.

- **JFAN1 / JFAN2 : CPU / SYS. Fan Connector**



PIN	DESCRIPTION
1	Ground
2	12V
3	Rotation Signal

3.10 VGA Connector

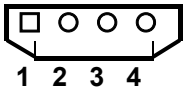
- **P3 : 15-pin Female Connector**

PIN	DESCRIPTION	PIN	DESCRIPTION
1	RED	2	GREEN
3	BLUE	4	NC
5	GROUND	6	GROUND
7	GROUND	8	GROUND
9	VCC / NC	10	GROUND
11	NC	12	DDC DAT
13	HSYNC	14	VSYNC
15	DDCCLK		

3.11 Power Connector

The PCISA-C3/EDEN SERIES is equipped with one standard power connector

- **CN10: 4-pin Connector**

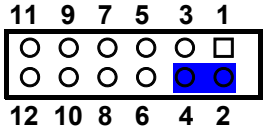


PIN	DESCRIPTION
1	+12V
2	GND
3	GND
4	+5V

3.12 External Switches and Indicators

There are several external switches and indicators for monitoring and controlling your CPU board. All functions are in the CN4 connector.

- **CN4 Pin Assignment and Functions :**



FUNCTION	PIN	DESCRIPTION	
SPEAKER	2	SPK SIGNAL	Jump for Buzzer
	4	Buzzer-	
	6	NC	
	8	VCC	
RESET	10	RESET	
	12	GROUND	
HDD LED	9	IDE_LED+	
	11	IDE_LED-	
POWER LED	1	LED+	
	3	LED-(GROUND)	
Reserved	5	GROUND	
	7	NC	

3.13 PS-ON Connector

This connector is used to control the ATX power supply.

- **CN9 : PS-ON Connector (please refer to Appendix D for details)**

PIN	DESCRIPTION
1	Ground
2	PS-ON
3	+5V Standby

3.14 LAN RJ45 Connector

The PCISA-C3/EDEN SERIES is equipped with dual Ethernet Controllers (Intel 82559 10/100Mbps, which are connected to the LAN via an RJ45 LAN connector. The pin assignments are listed in the following table:

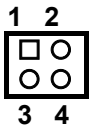
- **P1 LAN1 RJ45 Connector (10/100)**

PIN	DESCRIPTION	PIN	DESCRIPTION
1	TX+	7	N/C
2	TX-	8	N/C
3	RX+	9	Speed +
4	N/C	10	Speed -
5	N/C	11	Active/LINK +
6	RX-	12	Active/LINK -

3.15 External LED Connector

The LED connector includes Ethernet Link/Active LED, Ethernet speed LED.

- **CN1 External LED Connector**



LED -	LED +	LED Function
1	2	LAN LINK LED
3	4	LAN Speed LED

3.16 Compact Flash Storage Card Socket

The PCISA-C3/EDEN SERIES includes a slot for a Compact Flash Storage Card in IDE Mode(Using IDE 2).

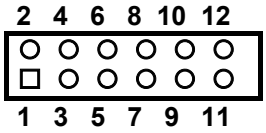
- **CN2 : Compact Flash Storage Card Socket pin assignment**

PIN	DESCRIPTION	PIN	DESCRIPTION
1	GROUND	26	CARD DETECT1
2	D3	27	D11
3	D4	28	D12
4	D5	29	D13
5	D6	30	D14
6	D7	31	D15
7	CS1#	32	CS3#
8	N/C	33	N/C
9	GROUND	34	IOR#
10	N/C	35	IOW#
11	N/C	36	OBLIGATORY TO PULL HIGH
12	N/C	37	IRQ15
13	VCC	38	VCC
14	N/C	39	MASTER/SLAVE
15	N/C	40	N/C
16	N/C	41	RESET#
17	N/C	42	IORDY
18	A2	43	N/C
19	A1	44	OBLIGATORY TO PULL HIGH
20	A0	45	ACTIVE#
21	D0	46	PDIAG#
22	D1	47	D8
23	D2	48	D9
24	N/C	49	D10
25	CARD DETECT2	50	GROUND

3.17 Audio Connectors

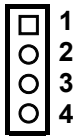
The onboard AC'97 CODEC supports several audio functions. The audio connectors are described below.

- **CN8:**



PIN	DESCRIPTION	PIN	DESCRIPTION
1	EAR OUT (LEFT)	2	EAR OUT (RIGHT)
3	GROUND	4	GROUND
5	LINE OUT (LEFT)	6	LINE OUT (RIGHT)
7	LINE IN (LEFT)	8	LINE IN (RIGHT)
9	GROUND	10	GROUND
11	MIC IN	12	GROUND

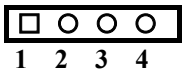
- **CD_IN1:**



PIN	DESCRIPTION
1.	CD SIGNAL (LEFT)
2.	GROUND
3.	GROUND
4.	CD SIGNAL (RIGHT)

3.18 RS422/485 Connectors

- **CN13:**



PIN	DESCRIPTION
1.	TX2+
2.	TX2-
3.	RX2+
4.	RX2-

Chapter 4. BIOS Setup

4.1 Introduction

This chapter discusses the Setup program built into the BIOS. which allows users to configure the system. This configuration is then stored in battery-backed CMOS RAM so that Setup information is retained whilst the power is off.

4.2 Starting Setup

The BIOS is immediately active when you turn on the computer. While the BIOS is activated, the Setup program can be entered in one of two ways:

1. By pressing <Del> immediately after switching the system on, or

2. by pressing the <Del> key when the following message appears briefly at the bottom of the screen during the POST (Power On Self-Test).

Press DEL to run SETUP.

4.3 Setup Summary

Standard CMOS Setup

Standard CMOS Setup to change time, date, hard disk type, etc.

Advanced CMOS Setup

Advanced CMOS Setup to configure system options.

Advanced Chipset Setup

Advanced Chipset Setup to configure chipset features.

Power Management Setup

Power Management Setup to configure power management features.

PCI / Plug and Play Setup

Configures PCI / Plug and Play features.

Peripheral Setup

Configures peripheral features.

Hardware Monitor Setup

Configures hardware monitor features.

Auto-Detect Hard Disks

Selecting these options allow the user to configure the drive named in the option. Select Auto-Detect Hard Disks to allow AMIBIOS to automatically configure the drive. A list of drive parameters the appears on the screen.

Change User Password

Change the user password.

Change Supervisor Password

Change the supervisor password.

Auto Configuration with Optimal Settings

Load configuration settings that ensure the highest performance.

Auto Configuration with Fail Safe Settings

Load fail-safe configuration settings.

Save Settings and Exit

Write the current settings to CMOS and exit.

Exit Without Saving

Exit without saving the current settings.

4.4 Main Menu Selections

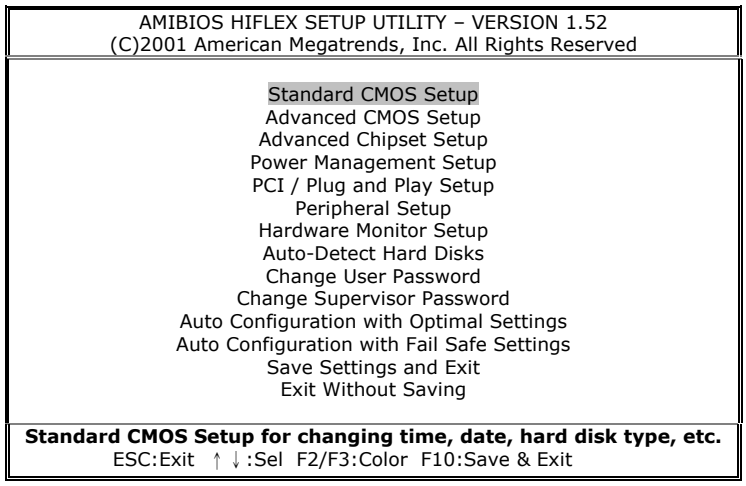


Figure 1:The Main Menu

4.5 Standard CMOS Setup Selections

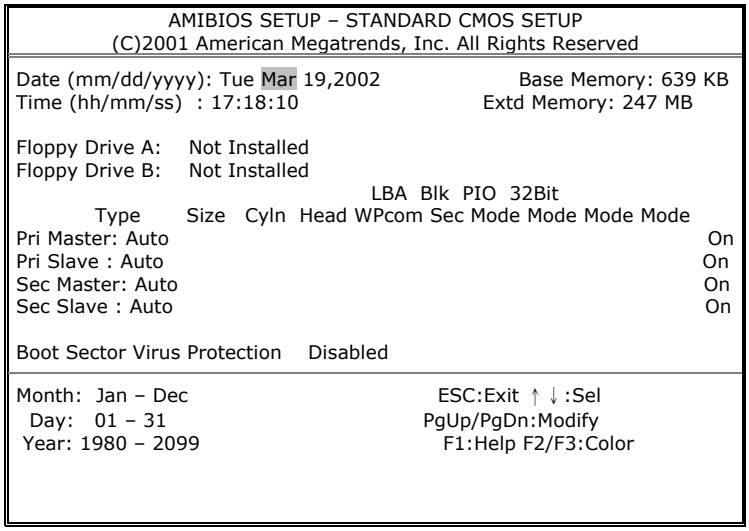


Figure 2:Standard CMOS Setup

Floppy A, B

Move the cursor to these fields and select the floppy type.

Primary/Secondary Master/Slave LBA Mode

LBA(Logical Block Addressing) is a new IDE HDD access method to developed to overcome the 528-megabyte capacity bottleneck. If your IDE hard disk capacity is greater than 528MB, AMIBIOS can enable this LBA mode feature. The option is only for Primary Master IDE LBA mode.

Primary/Secondary Master/Slave Block Mode

If your hard disk drive supports IDE block transfer mode, enable this option for a faster IDE hard disk drive transfer rate. The option is only for Primary Master Block mode.

Primary/Secondary Master/Slave PIO Mode

This option enables Primary Master IDE PIO mode on the IDE, which can set proper cycle timings. The cycle timing between the IDE PIO mode value and IDE cycle timing is shown below :
Mode 0 -> Timing (600ns)Mode 1 -> Timing (383ns)
Mode 2 -> Timing (240ns)Mode 3 -> Timing (180ns)
Mode 4 -> Timing (120ns)Mode 5 -> Timing (60ns)

Primary/Secondary Master/Slave 32Bit Mode

This option enables Primary Master IDE 32-bit data transfers on the IDE data port. If disabled,16-bit data transfer is used by the BIOS.32-bit data transfers can only be enabled if IDE prefetch mode is also enabled.

Boot Sector Virus Protection

When this option is enabled, AMIBIOS issues a warning when any program or virus issues a Disk Format command or attempts to write to the boot sector of the hard disk drive.

The Choice: Disabled, Enabled.

4.6 Advanced CMOS Setup Selections

AMIBIOS SETUP – ADVANCED CMOS SETUP
(C)2001 American Megatrends, Inc. All Rights Reserved

Quick Boot	Enabled	Available Options:
1st Boot Device	Disabled	Disabled
2nt Boot Device	Disabled	> Enabled
3rd Boot Device	Disabled	
Try Other Boot Devices	Yes	
S.M.A.R.T. for Hard Disks	Disabled	
BootUP Num-Lock	On	
Floppy Drive Swap	Disabled	
Floppy Drive Seek	Disabled	
PS/2 Mouse Support	Enabled	
System Keyboard	Present	
Primary Display	VGA/EGA	
Boot To OS/2	No	
Wait For 'F1' If Error	Enabled	
Hit 'DEL' Message Display	Enabled	
CPU MicroCode Updation	Enabled	
L1 Cache	Enabled	
L2 Cache	Enabled	ESC:Exit ↑ ↓:Sel
System BIOS Cacheabled	Enabled	PgUp/PgDn:Modify
C000 32K Shadow	Cached	F1:Help F2/F3:Color

Figure 3:Advance CMOS Setup

S.M.A.R.T. for Hard Disks

Self-Monitoring, Analysis and Reporting Technology. This option can help the BIOS to warn the user of a possible device failure and give the user a chance to back up the device before the failure actually happens.

The Choice: Auto, Disabled, Enabled.

Floppy Drive Seek

Set this option to Enabled to specify that floppy drive A: will perform a Seek operation at system boot.

The Choice: Enabled or Disabled.

Quick Boot

When Quick Boot is selected, DRAM testing function will be disabled.

1st Boot Device

This option sets the type of device for the first boot drives that the AMIBIOS attempts to boot from after AMIBIOS POST completes.

The Choice: Disabled, IDE-0, IDE-1, IDE-2, IDE-3, Floppy, ARMD-FDD, ARMD-HDD, CDROM, SCSI.

2nd Boot Device

This option sets the type of device for the second boot drives that the AMIBIOS attempts to boot from after AMIBIOS POST completes.

The Choice: Disabled, IDE-0, IDE-1, IDE-2, IDE-3, Floppy, ARMD-FDD, ARMD-HDD, CDROM.

3rd Boot Device

This option sets the type of device for the third boot drives that the AMIBIOS attempts to boot from after AMIBIOS POST completes.

The Choice: Disabled, IDE-0, IDE-1, IDE-2, IDE-3, Floppy, ARMD-FDD, ARMD-HDD, CDROM.

Try Other Boot Devices

Set this option to Yes to instruct AMIBIOS to attempt to boot from any other drive in the system if it cannot find a boot drive among the drives specified in the 1st Boot Device, 2nd Boot Device, 3rd Boot Device, 4th Boot Device options.

The Choice: Yes or No.

BootUp Num-Lock

When this option is selected, Num Lock is turned off when the system is powered on so the user can use the arrow keys on both the numeric keypad and the keyboard.

PS/2 Mouse Support

When this option is enabled, BIOS supports a PS/2- type mouse.

System Keyboard

This option does not specify if a keyboard is attached to the computer. Rather, it specifies if error messages are displayed if a keyboard is not attached. This option permits you to configure workstation with no keyboard.

The Choice: Absent, Present.

Primary Display

Select this option to configure the type of monitor attached to the computer.

The Choice: Monochrome, Color 40x25,Color 80x25, VGA/PGA/EGA, or Not Install.

Boot To OS/2

Set this option to Enabled if running OS/2 operating system and using more than 64MB of system memory on the motherboard.

The Choice: Disabled or Enabled.

Wait For 'F1' If Error

If this option is enabled, AMIBIOS waits for the end user to press <F1> before continuing. If this option is disabled, AMIBIOS continues the boot process without waiting for <F1> to be pressed.

The Choice: Disabled or Enabled.

Hit 'DEL' Message Display

Disabling this option prevents "Hit <DEL> if you want to run Setup" from appearing when the system boots.

The Choice: Disabled or Enabled.

System BIOS Cacheable

When this option is set to enabled, the System ROM area from F0000-FFFFF is copied (shadowed) to the RAM for faster execution.

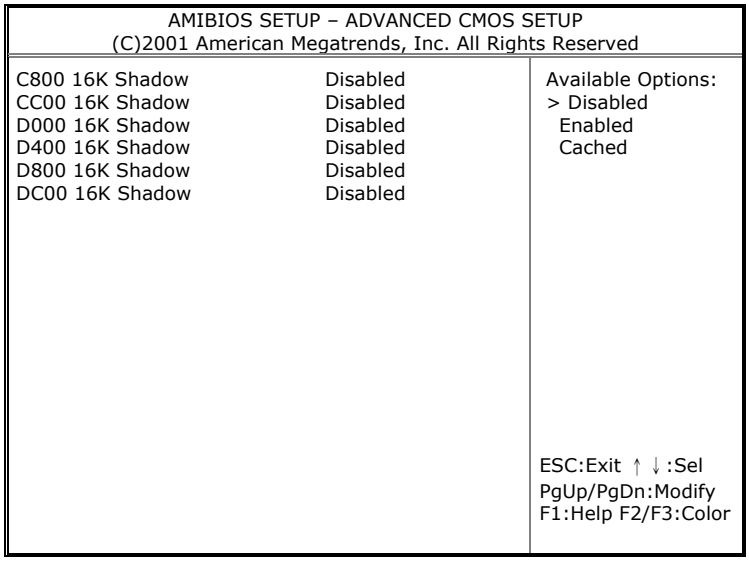


Figure 4: Advance CMOS Setup

C000,32k Shadow

When this option is set to enabled, the Video ROM area from C0000-C7FFF is copied (shadowed) to the RAM for faster execution.

- Disabled : The contents of the video ROM are not copied to the RAM.
- Cached: The contents of the video ROM area from C0000h - C7FFFh are copied from the ROM to

the RAM and can be written to or read from the cache memory.

- Enabled: The contents of the video ROM area from C0000h - C7FFFh are copied (shadowed) from the ROM to the RAM for faster execution.

C800, CC00, D000, D400, D800, DC00, 16k Shadow

These options enable shadowing of the contents of the ROM area named in the option title. The settings are Enable Disable, Cached.
The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards.

4.7 Advanced Chipset Setup Selections

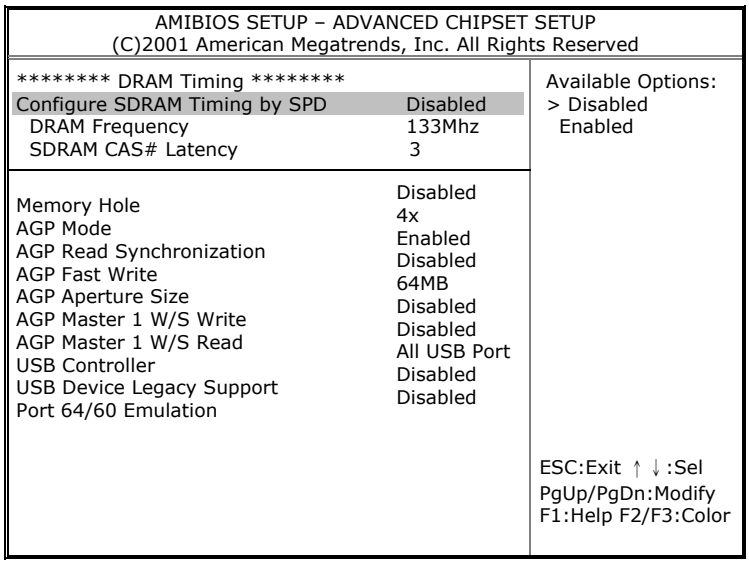


Figure 5: Advanced Chipset Setup

4.8 Power Management Setup Selections

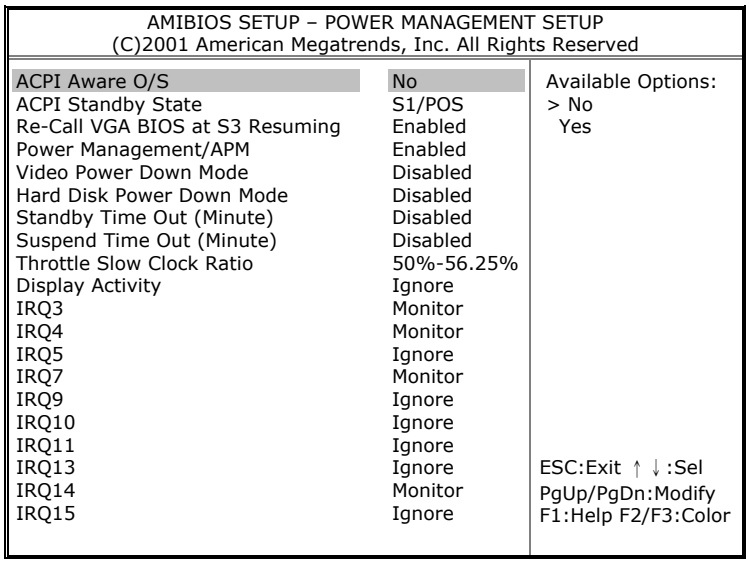


Figure 6: Power Management Setup

Power Management/APM

Set this option to Enabled to run APM (Advanced Power Management).

Video Power Down Mode

Set this option to Enabled to allow the BIOS to power down the Video adapter and Monitor.

Hard Disk Power Down Mode

Set this option to Enabled to allow the BIOS to power down the Hard Disk .

Standby/Suspend Time Out (Minutes)

This option specifies the amount of system inactivity (in minutes) before the system will enters Standby/Suspend state.

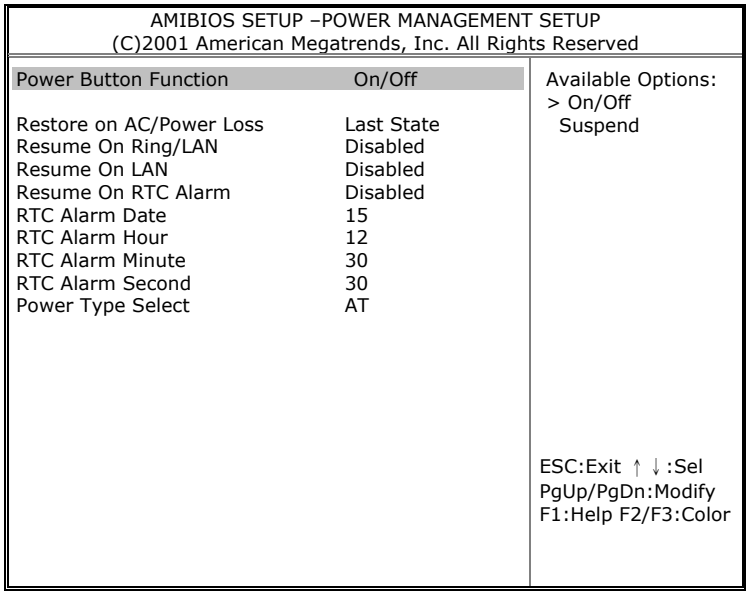


Figure 7: Power Management Setup

4.9 PCI / Plug and Play Setup Selections

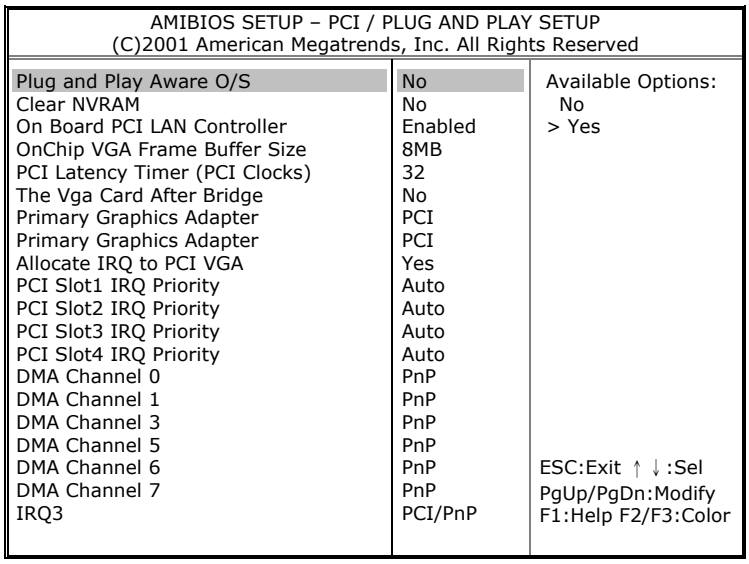


Figure 8: PCI / Plug and Play Setup

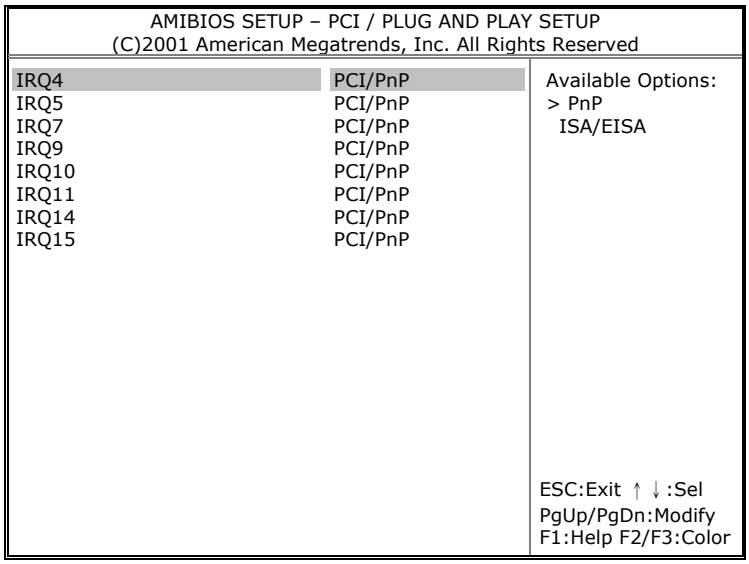


Figure 9: PCI / Plug and Play Setup

Plug and Play Aware O/S

If enabled, BIOS will configure only PnP ISA boot devices(i.e. all PnP ISA cards which have boot flag set). And PnP aware OS will configure all other devices. If disabled, BIOS will configure all devices.

DMA Channel 0, 1, 3, 5, 6, 7

The option allow the user to specify the bus type used by each DMA channel.

The Choice: PnP or ISA/EISA

IRQ3, 4, 5, 7, 9, 10, 11, 14, 15

The option specifies the bus that the specified IRQ line is used on. The user can reserve IRQs for legacy ISA adapter cards whilst determining if AMIBIOS should remove an IRQ from the pool of available IRQs passed to devices that are configurable by the system BIOS. The available IRQ pool is determined by reading the ESCD NVRAM. If more IRQs need to be removed from the pool, the user can optionally reserve the IRQ by assigning an ISA setting to it. Onboard I/O is configured by AMIBIOS. All IRQs used by onboard I/O are configured as PCI/PnP.

4.10 Peripheral Setup Selections

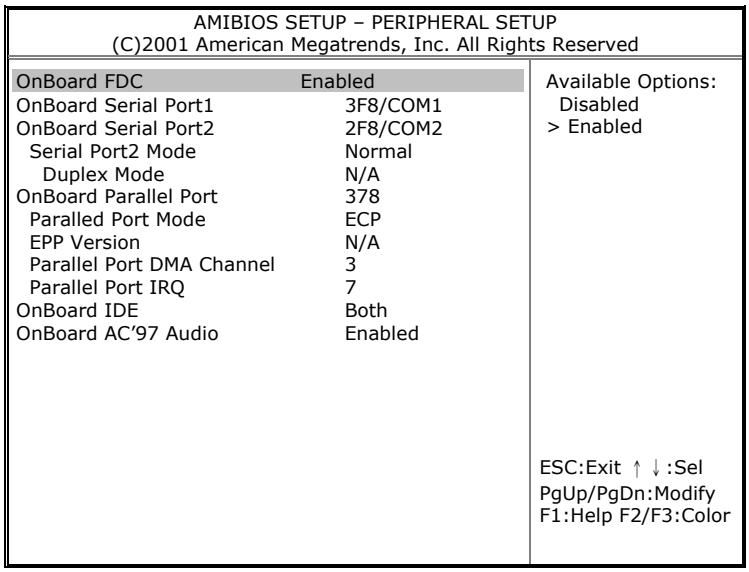


Figure 10: Peripheral Setup

On-Board Parallel Port

This option specifies the base I/O port address of the parallel port on the motherboard.

The Choice: Disabled, 378h, 278h, or 3BCh.

Parallel Port Mode

This option specifies the parallel port mode. The settings are Normal, Bi-Dir, ECP, EPP.

- Normal : The normal parallel port mode is used.
- Bi-Dir : Use this setting to support bi-directional transfers on the parallel port.
- EPP : The parallel port can be used with devices that adhere to Enhanced Parallel Port(EPP) specifications. EPP uses the existing parallel port signals to provide asymmetric bi-directional data transfer driven by the host device.

- ECP : The parallel port can be used with devices that adhere to Extended Capabilities Port (ECP) specifications. ECP uses the DMA protocol to achieve data transfer rates of up to 2.5 Megabits per second, and provides symmetric bi-directional communication.

Parallel Port IRQ

This option specifies the IRQ used by the parallel port.

The Choice: (IRQ)5, (IRQ)7.

Parallel Port DMA Channel

This option is only available if the setting for the Parallel Port Mode option is set to ECP. It sets the DMA channel used by the parallel port.

The Choice: DMA Channel 0, 1, or 3.

4.11 Hardware Monitor Setup Selections

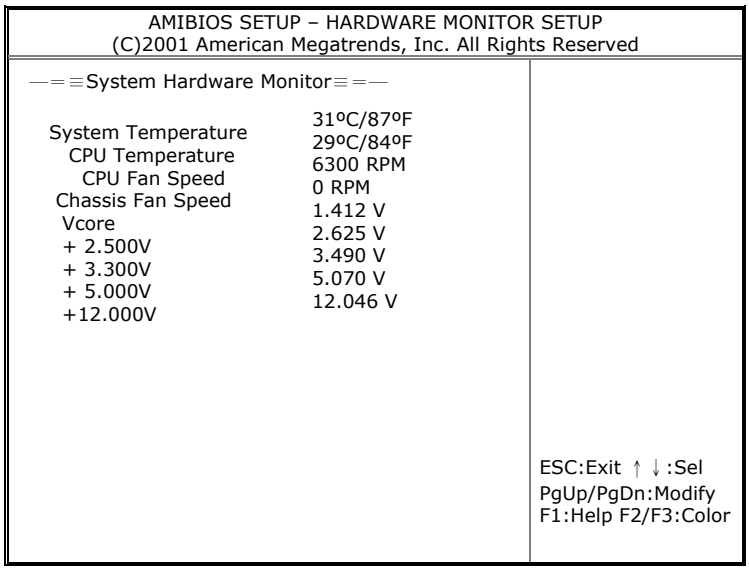


Figure 11: Hardware Monitor Setup

Appendix A. Watch-Dog Timer

The WatchDog Timer is a device which ensure that standalone systems can recover from abnormal conditions that cause the system to crash. These conditions may result from an external EMI or a software bug. When the system stops working, hardware on the board will perform a hardware reset (cold boot) to bring the system back to a functioning state.

Three I/O ports control the operation of WatchDog Timer.

443 (hex)	Write	Set WatchDog Time period
443 (hex)	Read	Enable the refresh the Watchdog Timer.
043/843 (hex)	Read	Disable the Watchdog Timer.

Prior to enabling the Watchdog Timer, the user has to set the time-out period. The range of the timer is 1 to 255 sec, set in increments of 1 second. The user will need to send the time-out value to the I/O port – 443H, and then enable it by reading data from the same I/O port. This will activate the timer that will eventually time out and check and monitor the CPU board. This must be done within the time-out period that is set by the software, For additional help, please refer to the example program. Finally, disable the Watchdog timer by reading the I/O port -843H or 043H - otherwise the system could reset unconditionally.

***Note**: A tolerance of at least 5% must be maintained to avoid unknown routines in the operating system (DOS), such as disk I/O that can be very time-consuming. Therefore if the time-out period has been set to 10 seconds, the I/O port 443H must be read within 7 seconds*.

Example Assembly Program:

```
TIMER_PORT   =  443H
TIMER_START  =  443H
TIMER_STOP   =  843H
;;Initial Timer Counter
MOV DX, TIMER_PORT
MOV AL, 8     ;;8 seconds
OUT DX, AL
MOV DX, TIMER_START
IN AL, DX.    ;;Start counter

W_LOOP:
MOV DX, TIMER_STOP
IN AL, DX
MOV DX, TIMER_START
IN AL, DX       ;;Restart counter
;;Add Your Application Here
CMP EXIT_AP, 0
JNE W_LOOP
MOV DX, TIMER_STOP
IN AL, DX
;;Exit AP
```

Appendix B. E2 Key™ Function

The PCISA-C3/EDEN SERIES provides an outstanding E^2KEY™ function for system integrators. Based on the E^2KEY™, ID Code, Passwords or Critical Data can be stored in the 1Kbit EEPROM. Because the EEPROM is non-volatile memory, you don't have to worry about losing important data.

The E^2KEY™ is based on a 1Kbit EEPROM which is configured to 64 words(from 0 to 63). The user can access (read or write) each word at any time.

When you start to use the E^2KEY™ the utility is already in the package. The software utility will include four files as follows,

README.DOC
E2KEY.OBJ
EKEYDEMO.C
EKEYDEMO.EXE.

The E2KEY.OBJ provides two library functions for the user to integrate in to their application with E^2KEY™ function. These library functions **(read_e2key and write_e2key)** are written and compiled in C language. Please check the following statement, in order to easily implement it.

unsigned int read_e2key(unsigned int address)
/* This function will return the E^2KEY™'s data at address. The address range is from 0 to 63. Return data is one word,16 bits

*/**void write_e2key(unsigned int address,unsigned data)**
/* This function will write the given data to the E^2KEY™ at a certain address. The address range is from 0 to 63. The data value is from 0 to 0xffff. */
To start using the function, please refer to the included EKEYDEMO.C code.

Appendix C. Address Mapping

IO Address Map

I/O address Range	Description
000-01F	DMA Controller #1
020-021	Interrupt Controller #1, Master
040-05F	8254 timer
060-06F	8042 (Keyboard Controller)
070-07F	Real time Clock, NMI Mask
080-09F	DMA Page Register
0A0-0BF	Interrupt Controller #2
0C0-0DF	DMA Controller #2
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F2	Core logic programming configuration
0F8-0FF	Math Coprocessor
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2 (LPT3)
2E8-2EF	Serial Port 4
2F8-2FF	Serial Port 2
300-31F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1 (LPT2)
3B0-3BF	Monochrome Display and Printer Adapter (LPT1)
3C0-3CF	Reserved
3D0-3DF	Color/Graphics Monitor Adapter
3E8-3EF	Serial Port 3
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1

1st MB Memory Address Map

Memory address	Description
00000-9FFFF	System memory
A0000-BFFFF	VGA buffer
C0000-C7FFF	VGA BIOS
F0000-FFFFF	System BIOS
1000000-	Extend BIOS

*Default setting

IRQ Mapping Table

IRQ0	System Timer	IRQ8	RTC clock
IRQ1	Keyboard	IRQ9	Available
IRQ2	Cascade to IRQ Controller	IRQ10	Available
IRQ3	COM2	IRQ11	Available
IRQ4	COM1	IRQ12	PS2 mouse
IRQ5	Available	IRQ13	FPU
IRQ6	FDC	IRQ14	Primary IDE
IRQ7	Printer	IRQ15	Secondary IDE

DMA Channel Assignments

Channel	Function
0	Available
1	Available
2	Floppy disk (8-bit transfer)
3	Available
4	Cascade for DMA controller 1
5	Available
6	Available
7	Available

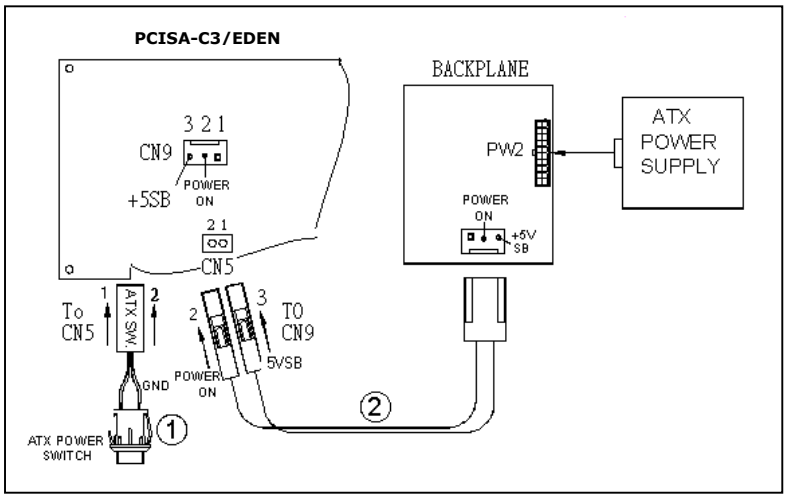
Appendix D. ATX Power Supply

The following notes show how to connect the ATX Power Supply to the backplanes and / or the ISBC card.

A. For backplanes with an ATX Connector

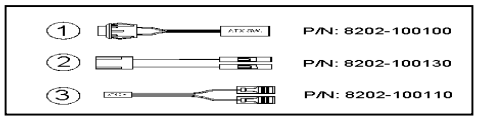
1. First disconnect the AC cord of the Power Supply from the AC source to prevent sudden electrical surge to the board.
2. Next, check the type of your CPU board. All CPU boards listed on the next page support ATX power supply but have two types of power switch connection:

- **PCISA-C3/EDEN SERIES (through Power Button & GND):**



Connect the ATX power button switch to the pin 1 (power button) and pin 2 of the CN5 on the board, and connect the power cable from backplane to CN9 of the CPU card.
If you want to turn ON the system, just press the button once.

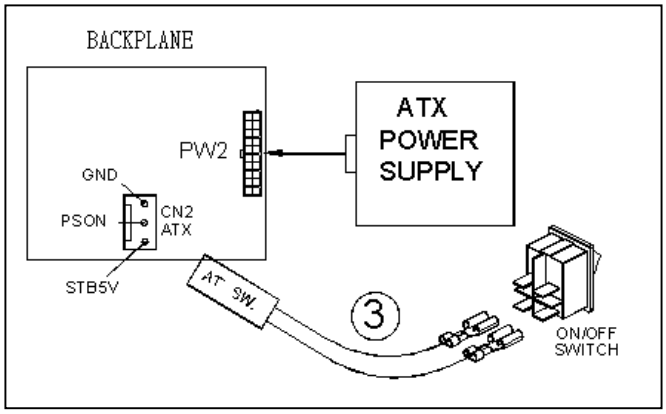
And If you want to turn off the power supply, please press the ATX power switch button for about 4 seconds.



For backplanes with an ATX power supply connector

For some SBC with no ATX power ON/OFF function, the user can control the ATX power supply via the backplane's PS ON connector. Refer to the figure below: for the backplanes with ATX connector, the connection can be made simply as follows:

1. Connect the ON/OFF switch to Pin 2 (PS ON) and Pin 1 (GND) of connector CN2
2. You may now turn the power On and OFF by using the power switch



Appendix E.
How to Use the Wake-Up Function

The PCISA-C3/EDEN SERIES provides two kind of Wake Up Function.
This page describes how to use the Modem Wake-Up and LAN Wake-Up functions.
Wake-Up function works whilst using ATX power supply,

- **Wake-Up By Modem Ring On**:
  In CMOS SETUP, the user must set the option ***Wake Up On LAN/Ring*** to enabled. The ATX power supply will be switched on when there is a ring signal detected on the pin "RI" of the serial port.

- **Wake-Up On LAN (for Intel 82559 LAN-chip)**:
  In CMOS SETUP, the user must set the option ***Wake Up On LAN/Ring*** to enabled. When the computer is in power-down status, a LAN Link/Active LED is flashing. This status indicates that the LAN chip has entered standby mode and is waiting for a Wake-Up signal. You can use other computers to wake up your computer by sending ID to it.

- **ID**: ID is the address of your system LAN. Every LAN chip has a factory- set ID which you can find it from network information in WINDOWS.

  ID's format is xx-xx-xx-xx-xx-xx
  Example ID: 00905C21D4D7